Multi-Sensing System for Parkinson's Disease Stage Assessment based on FPGA-embedded Serial SVM Classifier

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Abstract – The paper proposes a multi-sensing system for the jointly assessment of electromyographic (EMG) and electroencephalographic (EEG) signals for the neuromuscular syndromes progression assessment, such as the Parkinson's disease (PD). The architecture implemented on Altera Cyclone V FPGA, interfaces 8 wireless surface EMGs (lower limbs) and 7 wireless EEGs (motor-cortex). The acquired signals, digitized and pre-processed, underwent a time-frequency features extraction (FE), making data suitable for a Serial Support Vector Machine (SSVM) real-time classification.

The system has been in-vivo tested on 5 subjects (n=3 affected by mild PD and n=2 by severe PD). The experimental results showed an accuracy of ~94% in the pathology stage recognition, and near the 100% in distinguish healthy subjects from PD affected ones. The FPGA resources utilization results in: 31.04% ALMs, 15.87% registers, < 6% memory blocks and the 82.75% DSP blocks.

Keywords—Biosignals, FPGA, Wearable Diagnostic Platform, Cyber-Physical System

I. INTRODUCTION

The Parkinson's disease (PD) manifests as cardinal indicators, gait disorders such as: stride length, freezing of gait (FoG), trunk pendency, postural instability, bradykinesia [1].

At the state of the art, the only existing diagnosis is based on the physician expertise and the careful observation/evaluation of the subject parameters, while involved in outpatients clinical protocols.

In this context, several wearable solutions have been proposed in literature, aiming to support clinicians in performing diagnoses, differential analyses, and objective quantification of PD symptoms both in outpatient applications and in remote monitoring [1-5].Focusing on the innovate aspects, such as: the used technologies for sensing and computing, the monitored PD features, the platforms applicability, the adopted classifier and the linked accuracy, some solutions have been selected for a performance comparison.

Kostis et al. [1] used, as sensing node, the built-in accelerometer of a smartphone and the computational capability of the same device, to monitor the hand movement of healthy subjects and PD ones. Analyzing the tremor frequency, via Pearson coefficients-based classifier [1], they are able to reach the 90% of accuracy in healthy-PD differentiation.

In [2], Ruonala et al. exploit an accelerometer and wireless EMGs on brachii to monitor the tremor frequency features, and the muscular activities of the patients. They are able to differentiate, by using a threshold-based classifier, patients affected by essential tremors and patients affected by PD with an accuracy of 90.52%.

Salarian et al. [3] analyzed the difference between older healthy people and PD ones by monitoring the hand rotation via gyroscope connected to a microcontroller. They classified the difference by using a linear discriminant analysis (LDA) reaching the 94.2% of accuracy.

Finally, with the same goal (i.e. differentiate PD from older healthy subjects), Roeder et al. [4] analyze offline changes in human gait resulting from ageing or neurodegenerative diseases. They assess electrophysiological activity from EEG/EMG during treadmill and over ground walking. The pilot study does not provide a quantification of the accuracy degree in the discrimination.

A physiological study on the gait disturbances typical of the PD has been conducted by Günther at al. [5]. In their work [5], the authors propose a technique for characterizing leg muscle activation patterns via EMGs and the related changes in EEG activity during gait experiments. Specifically, they investigate the cortico-muscular synergies to prevent freezing-of-gait (FOG) episodes. At the moment this is a pilot study in the field and it is not implemented on any embedded device [5].

All the proposed solutions are able to reliably distinguish PD from healthy subjects (young and old), but the literature shows a lack of solutions for the quantitative differentiation between two contiguous PD stages (e.g., 3rd and 4th of the H&Y scale [6]).

Aiming to make finer the PD stages discrimination, in this work, the PD nature that involves motor and cerebral activities has been exploited [6, 8].

The paper outlines the design and the implementation of a technological tool for the PD progress differentiation, by analyzing the cortico-muscular implications in gait disorders.

For the purpose, the system has a sensing interface that wirelessly collects signals from 8 EMG signals and 7 EEG ones. The signals are synchronously digitized and analyzed in a real-time context. The processing consists of a time-frequency features extraction (FE) that defines the input of a Serial Support Vector Machine (SSVM) classifier, which has the role of discriminating two proven stage of the pathology: 3rd and 4th H&Y level [6].

The proposed platform has been tested on 5 patients under physician assistance (n=3 patients at 3rd H&Y stage and n=2 patients at 4th H&Y stage).

In the aim of a future ASIC implementation, the architecture has been validated on FPGA (Altera Cyclone V) resulting in a low utilization of resources (i.e., ~32% of the adaptive logic module, ~16% of the register and <6% of the available memory).

The paper is structured as follows: Sec. II briefly describes the medical background and the experimental protocol used during the system validation. Sec. III provides methodological details about the architecture Sec. IV briefly describes the FPGA implementation. Sec. V reports the experimental results and Sec. VI discusses the results, concluding the paper.

II. MEDICAL BACKGROUND AND EXPERIMENTAL PROTOCOL

The PD affects both motor and cerebral activities. Main cortical implications concern loss of automatisms in ordinary movements, due to the reduction of motor planning function capability [1, 6, 8-10]. They lead to abnormality in muscular behavior during gait patterns. The movement control capacity is managed, inter-alia, by cerebral processes known as Movement Related Potentials (MRPs) [7-11]. The here proposed system extracts time-frequency features of three MRPs: µ rhythms, β rhythms and Bereitschaftspotential (BP).

In particular, the BP is the direct responsible of the voluntariness in movement planning. Typically, it has its maximum about 200 ms before the opposite leg muscle activation onset. In frequency, it is detectable between 2 and 5 Hz.

The µ-rhythm has the role of movement actuation (i.e. the rhythm is suppressed after the movement end). Its synchronization (activation) and desynchronization (suppression) are visible, respectively, about 500 ms before the movement, and during the movement. It is recognizable in the band 7.5 Hz to 12 Hz. The β-rhythms are linked to the muscle firing management in the motor sequence. It operates in the band: 13 Hz - 40 Hz.

The MRPs are identifiable in the opposite hemisphere with respect to the limb involved in the gait phase of swing [7, 9].

The signals analyzed in the following were acquired and computed in real time in the neurology department of the local hospital. Here, the subjects were asked to perform a standardized task, prescribed by the Unified Parkinson Disease Rating Scale (UPDRS) [10]: the 10-meter walk.

III. THE ARCHITECTURE

An overview of the implemented system is shown in Fig.1. Specifically, the architecture can be divided into two main blocks: the Acquisition System and the Computing one. As shown in Fig.1, the first block comprises the EEG and EMG sensor nodes distributed on the head and on the lower limbs of the patient under test, while Computing System consists of the algorithm (pre-processing, feature extraction (FE) and classification) implemented on the Altera Cyclone V FPGA.

A. The Acquisition System

The acquisition system (i.e., EEG and EMG in Fig.1) consists of a 32-channel EEG headset (g.Nautilus Research by g.Tec) and 8 wireless differential surface EMG (Cometa Wave Plus by Cometa S.r.l) [11]. The acquisition system transmits, via IEEE 802.15.4 protocol, the data acquired from 7 EEG sites along the sensory-motor area: T3, T4, C3, C4, CZ, P3, P4. The AFz electrode is used as GND for a monopolar reading and the right ear lobe is the reference electrode (REF). EEGs are recorded with 24bit resolution at f_s=500Hz sampling rate (analog input range: ±375mV).

In a synchronous manner, 8 surface EMG channels have been monitored from following bilateral muscle groups: Anterior Tibialis (AT), Lateral Gastrocnemius (LG), Rectus Femoris (RF), and Biceps Femoris (BF). The EMG signals are recorded with a sample rate of 2048 Hz and down sampled to 500 Hz (16-bit resolution) to match the EEG signal sampling frequency [11].

The EEG/EMG equipment is compliant with the wearability constraints [9] and allows a continuous monitor for about 11 hours with a delay in digitization and transmission of 14 ms [11].

Pre-processing. EEG and EMG signals have been collected from two synchronized gateways interfaced with the DE1-SoC board that contains the FPGA. Recorded signals are initially filtered as follows:
- **EEG.** The EEGs are progressively band-filtered between 1 Hz and 40 Hz, before the transmission, by using a built-in 8th order Butterworth IIR filter.
- **EMG.** Also the surface EMGs are high passed, before the transmission, with a provided 4th order Butterworth IIR filter with cut-off frequency at 10 Hz.
- A numeric notch filters 48-52 Hz was implemented for both EEG and EMG signals.

B. The Muscle-based Trigger

The acquired EMG signals undergo a preliminary processing: the "Muscle-based Trigger" procedure (Fig 1). It consists in "translating" a 16-bit EMG signal in a square waveform.

The trigger signal can assume '0' or '1' according to the muscle activation condition. This condition is realized by using dynamic
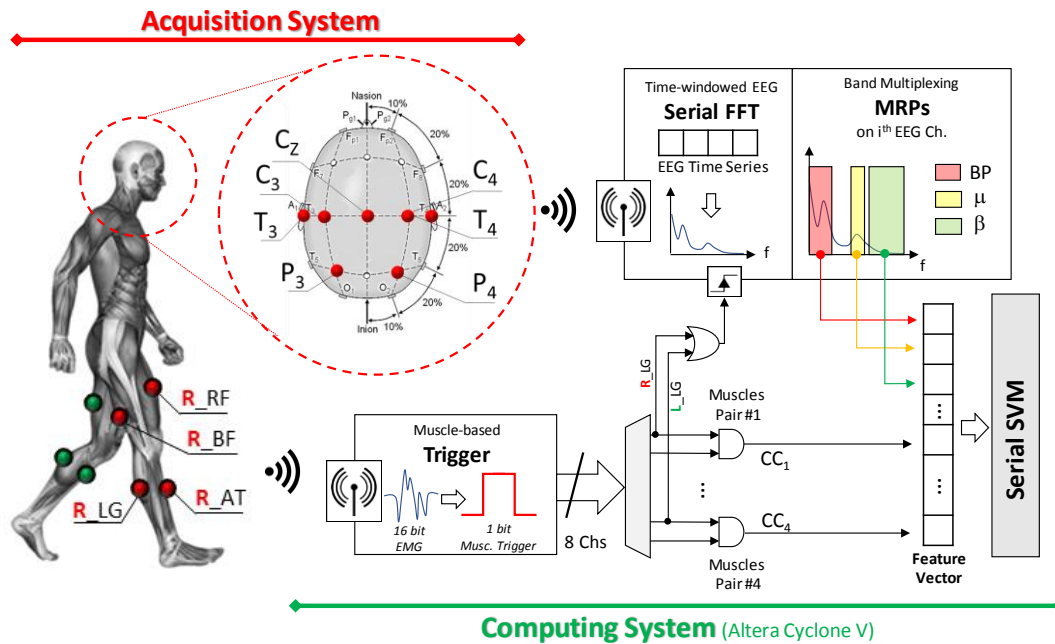

Fig. 1. Overview of the system implemented on FPGA from the biosignals (i.e., EMG, EEG) acquisition to their Serial SVM based classification. For the sake of readability, the figure shows, in details, only the names from the right leg electrodes.

average-based threshold algorithm, previously treated in [9, 11]. Briefly, each squared EMG sample is stored in two shift registers. The first register stores 512 samples (i.e., ~1 s of acquisition) which are used to compute the mean signal power, namely global average (GA). The GA works as the dynamic threshold. The second register stores the last 256 samples previously collected (i.e., 500 ms of acquisition) and are used to compute again the average of the signal power, namely local average (LA). Then the LA and GA are compared. For the i-th sample, the muscle is considered contracted if LA>GA. This process is cyclically updated sample-by-sample, each 2 ms.

Eight square waveforms are derived by the above-described trigger generation procedure, one per each monitored muscle. The muscles are then paired as agonist-antagonist couples and sent to common AND gates. For example, the right lateral gastrocnemius (R_LG) and the right anterior tibialis (R_AT) binary waveforms are sent, in parallel, to a AND gate providing as an outcome the co-contraction waveform for the considered pair (i.e., CC1 in Fig.1). According to Fig. 1, the considered pairs are R(L)_LG-R(L)_AT, R(L)_BF-R(L)_RF.

C. The EEG Computing

The cortical analysis is enabled every time the rising edge of a trigger from gastrocnemius (i.e., R_LG or L_LG) occur.

The raw EEG acquired from the dedicated motor cortex are processed by the "Time-window EEG Serial FFT" and the "Band Multiplexing MRPs" blocks in Fig.1. The first block applies a 32-bit words radix-2 Fast Fourier Transform (FFT) [9, 11] to an EEG subset composed of the 256 samples before the trigger onset (i.e. ~500 ms of acquisition).

The frequency resolution of the FFT is 2 Hz, enough for the band multiplexing [11] implemented by the second block in Fig.1 (i.e., Band Multiplexing MRPs). Once the FFT is completed the MRPs values are extracted from the spectrogram, returning the power spectrum density (PSD) in the BP, μ and β bands for each evaluated channel [7, 9, 11].

D. The SSVM Classifier

The EEG and EMG computing branches outcomes (i.e., BP, μ and β bands PSD for each channel and the LG-TA and BF-RF co-contractions timing) formally represent the features that will be used for the discrimination of the 3rd and 4th PD stages according to the H&Y rating scale [6].

For the PD stages discrimination, it has been chosen a Support Vector Machine (SVM classifier). Indeed, the SVM allows the system to learn by small set of observations and no need accurate FE stage [12].

To train an SVM, in a supervised way, a set of labelled features vectors (LFV) are needed.

The LFV has the form: {$\mathbf{F}i \in \Re^{Nf}$, Li}, where i=1…N_{obs} is the number of observations that compose the SVM *training dataset,* and N_f is the number of features (EEG and EMG branches outcomes). $\mathbf{F}i \in \Re^{Nf}$ is the features vector related to the i-th observation, and in analog manner Li∈ {−1, 1} is the i-th observation label: Yi=-1 → 4th stage of PD, while Yi= 1 → 3rd H&Y stage.

In its linear form, the SVM derives the hyperplane that maximize the distance between the closest negative and positive labelled points. The points related to the two classes that fall inside this maximal distance are named *support vectors* (SV). The matrix

$SV \in \Re^{Ns,Nf}$, with Ns number of support vectors (Ns<<N_{obs}), contains all the points inside the tolerance and the same length of the LFV. Each support vector is linked to a dedicated label, named $L_j \in \{−1, 1\}$ and a Lagrange multipliers α_j.

According to [12], the general SVM prediction function is:
$$f(x) = \sum_{j=1}^{Ns} \alpha_j Y_j \cdot k(x, SV) + b \qquad (1)$$

where x is the features vector to be labelled (or predicted): unlabeled feature vector (UFV); b is the SVM bias term, and $k(x, SV) = x^T SV$ is the linear SVM kernel function [12].

In order to ensure a quick time prediction, the proposed system optimizes the vectors labeling, classifying the features in a chronological order. In fact, not all the features are sent to the classifier at the same time, but they follow a computation sequence that determines the chronological order.

Considering the UFVs and the SV as a time continuous signals, refreshed by the variable computing time step t_i, the SVM prediction formula can be simplified as:
$$f(x) = (\sum_{j=1}^{Ns} \alpha_j L_j \cdot \sum_{i=1}^{Nf} x(t_i) \cdot SV_j(t_i)) + b \qquad (2)$$

where t_i is the arrival time of the i-th features.

Due to its time-continuous nature, the proposed SVM is named in the following: Serial SVM (SSVM).

It is important to note that a classic SVM (eq.(1)) needs to collect all the features before to compute N_s dot products and N_s-1 sums for the prediction [12]. In the SSVM, the dot products are done in a time- continuous" way (i.e., once the inputs $x(t_i)$ occurs). Thus, in terms of prediction timing, the worst case of the SSVM is always better than the best case in the classic SVM.

The implemented classifier is based on a hybrid approach: the MATLAB®2017a/Simulink environment realizes the off-line training stage, ensuring a compromise between classification accuracy and number of support vectors to be implemented on FPGA (≤ 15 support vectors) for the on-line phase. This solution avoids introducing on FPGA the computational complexity linked to the SVM learning.

Data that compose the training dataset have been acquired via FPGA (to minimize the approximation error) and offline used to characterize the SSVM. The extracted parameters (i.e., SV_s, α_s, Y_s) compose a memory initialization file (MIF- *SVM configuration file*) stored in a FPGA ROM for the real-time use. The Fig. 2 shows the working principle of the SSVM, by using 2 blocks of (SV_s, α_s, Y_s) and b.
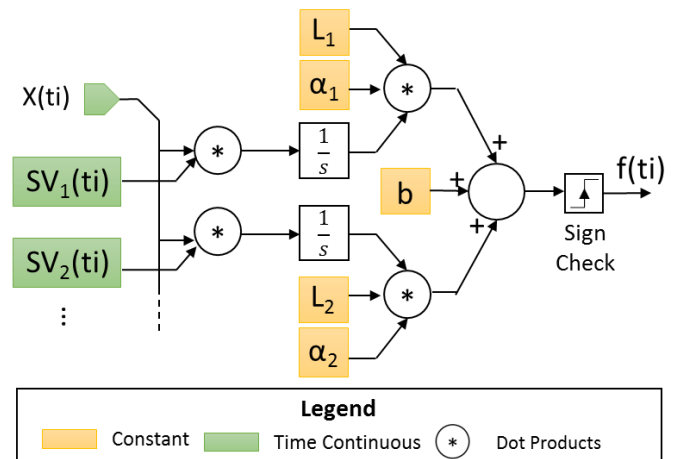

Fig. 2. SSVM working principle. The details are reserved to the first two support vectors parameters (SV_s, α_s, Y_s)

IV. The FPGA Implementation

The above-described system has been implemented on an Altera Cyclone V SE 5CSEMA5F31C6N FPGA, via VHDL coding, according to [9, 11, 12]. The system I/O interface is characterized by 15 inputs (i.e., EEG/EMG) and a flag in output (i.e., '-1' if the patient under test is classified as 3rd H&Y stage, or '1' if the patient is classified as 4th stage of H&Y scale).

The chosen system clock is 8MHz (derived through a PLL from the embedded 50MHz FPGA clock), while a 500Hz clock (500Hz_Clk) is derived by the system clock to manage the new data (EEG/EMG) arrivals.

A. The Muscle-based Trigger Implementation

The Altera Cyclone V implementation of the muscle-based trigger has been widely treated and analyzed in our previous works [9, 11]. The works provide complete details about its application. For the specific application, we designed two parallel VHDL FSMs, which provide the GA (threshold) and the LA, as defined in Sec. III.B. The two FSMs are supported by 2 dedicated RAMs: the GA one with M=512 words of 32bit (~1s), and the LA one that exploits N=128 words of 32bit (~250ms). The comparator in output (GA>LA) defines the 1-bit EMG trigger, used both as trigger for the EEG computing and for the co-contraction calculation. The co-contractions waveform is computed conducting both agonist and antagonist muscle triggers to an AND gate. When high, this waveform enables a dedicated counter that increases by a *module 2* at each 500Hz_Clk rising edge, providing the co- contraction times in ms.

B. The EEG Computing Implementation

The management circuitry for the EEG computing path implements a single *FFT processor* (256 points - 24bit resolution), based on a radix-2 butterfly structure, sequentially fed with the data provided by seven different EEG branches.

In particular, 256 samples (i.e. 500ms of acquisition, for each EEG channel), are cyclically stored in 256 words of 24 bits RAMs (one per each channel) to be analyzed, waiting for the proper trigger. The RAMs that contain the EEG data are driven in a FIFO-like functionality (i.e., circular memories).

When activated by the LG trigger, the cortical evaluation system provides the data to be analyzed via FFT, and the FFT clock (*FFT Clk*).

In particular, the RAMs operate with a 5*00Hz_clk* for the register filling management but the *FFT processor* uses a 4MHz clock (*FFT Clk*) for the internal operations.

When the rising edge of the Gastrocnemius trigger occurs, the system start sending data, channel-after-channel, to *FFT processor* via dedicated MUX. In this way, it is possible to serially analyze seven EEG chunk with a single *FFT Processor* reducing the resources consumption. The *FFT Processor* outcomes are sent to an MRPs extraction block, and the FSM is reset. When the FFT is over, the processor set a flag to '1' that means waiting for the new set of EEG samples. Contextually, this flag enables a 3-bit address counter (i.e., 7 channel), which drives the MUX in channel selecting. The MRPs calculation FSM extracts the BP, μ and β in a sequential way realizing a "time continuous" signals.

C. The SVM Classifier

The FPGA implementation of the SSVM (simplified in Fig. 2) is shown in Fig. 3.a.

The classifier operates downstream of the EEG and EMG branches. Considering a single reference leg movement (e.g., left), the classification block organizes the MRPs and the co-contractions in a time continuous feature signal structure, the **UFV**$\in \Re^{B,Nf}$ in Fig.3.a, where B is the number of bits that compose the sample (B=12 bits) and N_f is the number of features (N_f=25).

For sake of clarity, Fig. 3.a details a single computation block (i.e., it considers **SV1** and linked parameters), even if 15 similar blocks operate in parallel following the same procedure.

These blocks, which proceed the final sum, are named Weighted Sums ($W\sigma_j$) and exploit the previously trained SVM parameters: $\{\alpha_j, SV_j, y_j\}$. These parameters are stored in a dedicated 45 words ROM, via memory initialization file (*SVM Config.*).

In particular, the system synchronically manages the SV_j, as time continuous signal timely matching it with the UFV streaming (as shown in Fig.3.a with the green and red time-series).

The $SV_j(t_i)$ and the $UFV(t_i)$ are multiplied generating the signal $UFV(t_i) \cdot SV_j(t_i)$, then integrated by a cumulative sum based on a D-FF. The resulting signals is the σ_j that multiplied by the corresponding Lagrange multiplier, α_j, and the dedicated support vector label L_j provides a weighted σ_j ($W\sigma_j$).

This latter signal, provided by all the weighted sum blocks, leads to the prediction ($f(x(t_i))$) by a general sum in which converge all the WS_j with j=1…15 and the SVM bias (b). Then a zero-threshold comparator (*Sign Check*) determines the label assignment for the patient classification. Fig.3.a shows a simplified RTL view of the SSVM implementation, focusing on a single weighted sum. The panel 3.b shows the system resource utilization and Fig 3.c analyzes with a colormap the wire utilization.
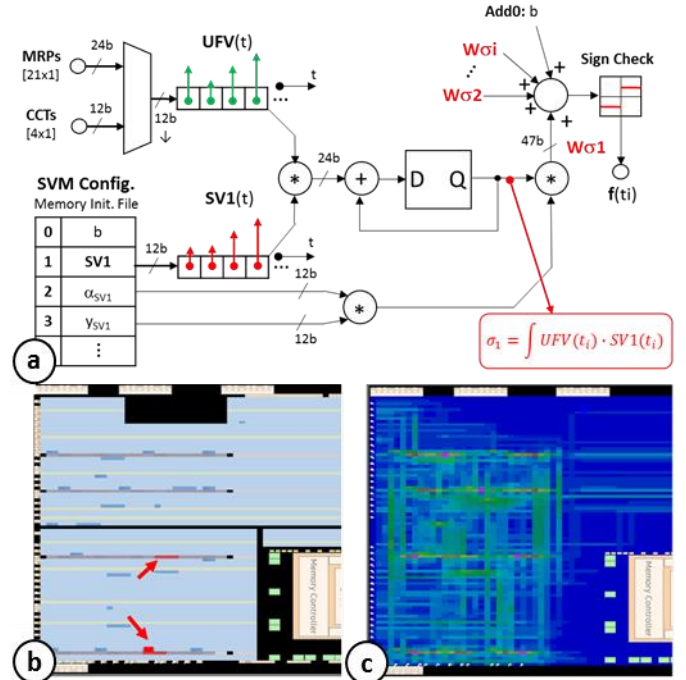

Fig. 3. SSVM classifier implementation: (a) simplified RTL for a single Weighted Sum block (b) FPGA resource utilization of a WS_j (c) Routing utilization of the SVM Classifier

V. Experimental Results

This paper outlines the experimental validation of the classification system, through in-vivo measurements on a dataset that includes EEG/EMG recordings from n=3 subjects affected by mild form (3rd H&Y stage) of PD and n=2 subjects in severe state of PD (4th H&Y stage). The patients have been previously classified in this way by highly specialized medical staff, which selected the subjects to be analyzed with standard protocols [10]. The subjects under test were involved in a 10-meters walking task, collecting respectively about 2600 steps per patient in 8 independent runs. Each subject is asked to perform a separate validation run of 200 steps.

A. Off-line Machine Learning Stage

The off-line side of the classifier realized a supervised ML stage on a dedicated training dataset, realized by merging about 2600 steps per patient, for a total of about 13000 steps. The dataset has been reduced and offline balanced in random way (5000 steps for the 3rd H&Y stage patients and the same number for the 4th stage ones).

The SVM hyperplanes extraction has been realized with Steve Gunn's approach [12]. The SVM training was done by using the cross-validation method (with 30 folds), protecting the trained model against overfitting by partitioning the dataset into folds and estimating the accuracy on each fold.

The resulting classifier reached an accuracy of 97.21% in a supervised cross-validation test, asking for 4.86s ±1.6 s.

B. The Real-time Classification Stage

The validation run steps have been used for the assessment of the SSVM real-time accuracy. The validation has been conducted on 345 observations from mild PD subjects (3rd H&Y) and 211 from heavy PD affected ones (4th H&Y).

In the real-time validation context, the implemented classifier shows an overall accuracy of 93.82% with a positive predicted value rate of 93.33% (322/345) for the 3rd stage subjects and the 94.31% (199/211) for 4th stage ones.

C. Altera Cyclone V Resources Utilization

During the in-vivo measurements, the system involves approximately 90kbps, providing in output a Boolean flag each step. Also, the implemented system uses 9957/32070 ALMs (31%), 237876/4065280 memory blocks (5.85%), 10180/64140 registers (15.9%) and 72 DSP blocks (82.7%).

Fig.4 shows detailed the percentage of the used resources requested by the operating entities.

VI. Conclusion

In this paper has been proposed the design, implementation on FPGA and in-vivo test of a time-continuous classifier for the PD progression detection. The discrimination concerns the recognition of two clinical proven PD stages, not so far among each other in term of symptoms. The proposed system exploits and numerically analyzes signals from wearable EEG and surface EMG. The bio-signals classification is firstly entrusted to an innovative neuromuscular FE stage operating synchronously with the gait. Finally, the extracted features are classified through a serial version of SVM.
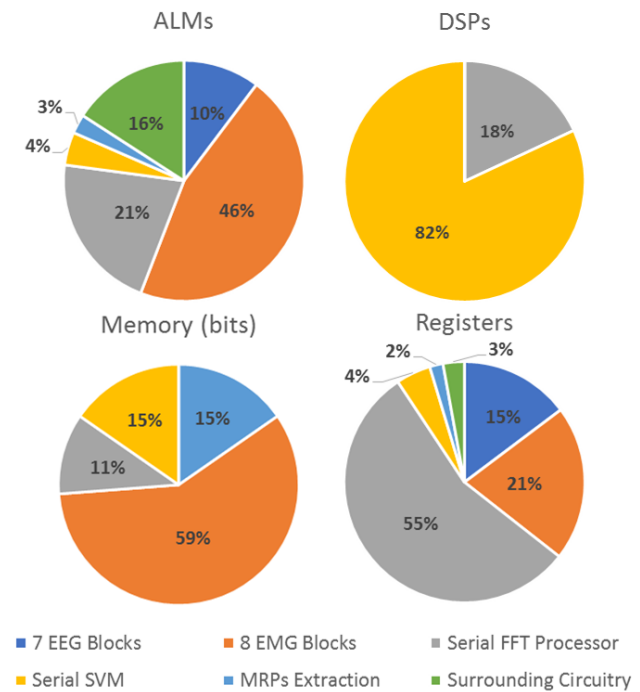

Fig. 4. Details of FPGA resources utilization in terms of ALMs, DSPs, Registers and Memory blocks

The digital architecture for the real-time classification has been fully implemented and validated on Altera Cyclone V FPGA.

In-vivo measurements, on 5 subjects, validate the classification accuracy requests, reaching about 94%.

The FPGA-based prototyping showed a general low utilization of the available resources (i.e., ~32% of the adaptive logic module, ~16% of the register and <6% of the available memory) demonstrating that an ASIC implementation of the algorithm is feasible. The FPGA prototype acknowledges an ASIC design but even at this development stage, it represents a breakthrough in the field of the PD progression stage recognition.

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